泰芯半导体
TaiXin Semiconductor

TXW817 Datasheet

Taixin Semiconductor Co.,Limited

3rd Floor, Gang 11 Building, 1st Jin Tang Road, Hi-tech Zone, Zhuhai China.

Liability and Copyright

Limitation of Liability

THIS DOCUMENT IS INTENDED FOR REFERENCE ONLY. Zhuhai Taixin Semiconductor Co,. Ltd (hereinafter referred to as "Taixin") does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Taixin reserves the right to make corrections, enhancements, and other changes to this document without notice.

Taixin assumes no liability for applications assistance or the design of customers' products. **Customers are solely responsible for the design, validation, and testing of its applications as well as for compliance with all legal, regulatory, and safety-related requirements concerning its applications.**

Taixin shall not be responsible for any damages, costs, losses, and/or liabilities arising out of customer's non-compliance with this section; concurrently, Customer will fully indemnify Taixin against any damages, costs, losses, and/or liabilities arising out of customer's non-compliance with this section.

Copyright Notice

Without the the written consent of Taixin, no party shall modify, adapt, alter, translate, or create derivative works from this document for commercial purposes.

Without the written consent of Taixin, no party shall disclose or distribute any or parts of the source code, SDK, binaries and object code mentioned in this document to any third party.

No party shall modify, reverse engineer, disassemble, decompile or otherwise attempt to discover the source code of any non-source code parts of the SDK including, but not limited to pre-compiled binaries and object code.

Furthermore, any other actions that may infringe upon Taixin's rights or other intellectual property owners are strictly prohibited.

For the subject who commits the above infringement, Taixin has the right to take necessary legal measure in accordance with the laws of the People's Republic of China or other applicable laws and international treaties, including but not limited to filing a lawsuit or arbitration against the infringer, or applying for legal compulsory measures.

Zhuhai Taixin Semiconductor Co., Ltd.

September 24,2024

Revision History

Date	Version	Revision Notes	Reviser
2025-02-27	V1.0	Initial version	TX

Table of Contents

1. Product Overview

1.1. Description

The TXW817 is a low-power, high-performance, highly integrated 2.4GHz Wi-Fi + BLE multimode IoT SOC chip. It integrates the IEEE 802.11 b/g/n baseband and RF (Radio Frequency) circuits, including the power amplifier PA (Power Amplifier), low noise amplifier LNA (Low Noise Amplifier), RF balun, antenna switch, and power management module.

The TXW817 Wi-Fi baseband implements OFDM (Orthogonal Frequency Division Multiplexing) technology and is backward compatible with DSSS (Direct Sequence Spread Spectrum) and CCK (Complementary Code Keying) technologies. It supports the IEEE 802.11 b/g/n protocol, with support for 20MHz standard bandwidth and 5MHz/10MHz narrow bandwidth, providing a maximum physical layer rate of 72.2 Mbit/s.

The TXW817 chip integrates a high-performance 32-bit microprocessor with built-in MJPEG (supporting VGA/720P). It provides a rich set of peripheral interfaces, including DVP, LCD, USB 2.0 High-Speed Host/Device (Host supported in some packages), SDMMC Host, SDIO 2.0 Slave, RMII MAC, SPI Master & Device, UART, IIC, IIS, PDM, IR Send/Receive, PWM, GPIO, and general-purpose and audio ADC/DAC. It also supports running programs on SPI Flash. The chip supports RTOS and third-party components and comes with an open and user-friendly development and debugging environment.

The TXW817 series includes multiple models and offers the mainstream QFN48 packaging option. Depending on the packaging form, the peripheral resource allocation in the device may vary. Some packages support integrated PSRAM and Flash.

Application :

- Wireless audio and video applications
- MiniDV
- IPC

1.2. Features

- **Wi-Fi MAC & PHY**
  - Supports IEEE 802.11 b/g/n standards.
  - Supports 1T1R mode with data rates up to 72.2 Mbps.
  - Excellent transmission power and reception sensitivity.
  - Integrated PA, LNA, and RF switch.
  - Supports STA, AP, AP+STA (repeater), and STA+STA functions.
  - Frame aggregation (TX/RX A-MPDU, RX A-MSDU).
  - Supports RX STBC (Space Time Block Coding).
  - Supports WPA/WPA2/WPA3.

- **BLE**
  - Supports Bluetooth fast pairing.
  - Supports coexistence of Wi-Fi and BLE.

- **Video**
  - Supports video data sources from DVP, UVC, and SPI lens inputs.
  - 1 MJPEG encoder with maximum resolution support: 1920×1080 @ 30fps.
  - 1 MJPEG encoder/decoder with maximum resolution support: 1920×1080 @ 30fps.
  - Supports timestamp watermarking, color framing, motion detection, and optical flow algorithm hardware acceleration.

- **Audio**
  - Supports single-ended and differential input high-performance analog microphones with built-in PGA.
  - 1 delta-sigma audio ADC.
  - 1 delta-sigma audio DAC.
  - Supports sampling rates of 8/11.025/12/16/22.05/24/32/44.1/48 kHz.

- **LCD**
  - Supports RGB interface, MCU8080 interface, and MCU6800 interface for LCD screen display.
  - Supports image scaling, 90/180/270-degree rotation, and horizontal and vertical mirroring.
  - Supports image OSD (On-Screen Display) and alpha blending.
  - Supports CCM (Color Correction Matrix), gamma correction, saturation, and contrast adjustment.

- **MCU**
  - CK803 CPU with a maximum clock frequency of 240 MHz.
  - 272 KB SRAM.

- Supports external crystal oscillators of various frequencies and supports sharing crystal input with the system master control chip.
- Supports RTC (Real-Time Clock).
- Supports 32 kHz crystal oscillator.
- 17 timers:
  - 1 always-on domain 32-bit timer.
  - 4 low-power mode 16-bit timers, supporting hardware low-power breathing light function.
  - 8 32-bit timers.
  - 2 16-bit timers, supporting infrared transmission/reception and LED strip drive.
  - 1 24-bit system tick timer.
  - 1 RTCC (Real-Time Clock Calendar) timer.
- Supports ULP (Ultra-Low Power) and LP (Low Power) low-power modes. ULP mode current < 28 μA @ 25° C, supporting multiple I/O wake-up.
- Built-in temperature sensor.
- Built-in LVD (Low Voltage Detection).
- Built-in watchdog timer.
- Built-in multiple LDO outputs with voltage range of 1.8 – 3.3 V.
- 48-bit unique chip ID (UID).

- Peripherals
  - 31 programmable GPIOs, supporting edge or level-triggered interrupts.
  - 1 12-bit ADC, which can be multiplexed as a DAC.
  - 1 12-bit analog comparator.
  - 1 QSPI, supporting external SPI FLASH and PSRAM.
  - 1 CMOS Sensor 8-bit DVP, with interface supporting up to 120 MHz.
  - 1 Motion JPEG encoder.
  - 1 Motion JPEG encoder/decoder.
  - 1 LCD.
  - 2 I2S/PCM.
  - 1 PDM.
  - 1 SDIO 2.0 High-Speed Device.
  - 1 SD Host Controller.
  - 1 USB 2.0 High-Speed Device.
  - 3 SPI interfaces (Master/Slave), with 2 configurable as I2C Master/Slave.
  - 3 UART interfaces (1 supporting flow control and RS485).
  - 1 infrared transmitter and multiple receivers.
  - 14 PWM outputs (multiplexed with timers), including 4 independent 16-bit PWMs, supporting low-power mode PWM.

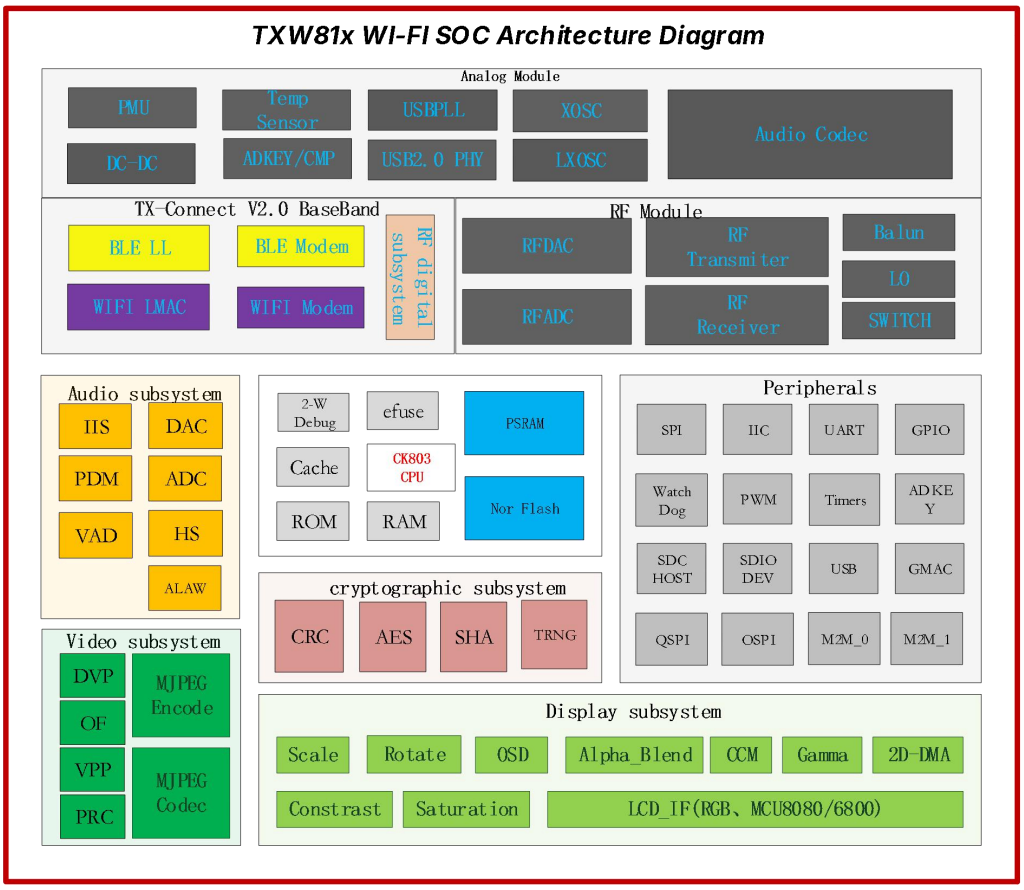
- Boot Interfaces
  - SDIO2.0 Device, USB2.0 Device, SPI Slave, UART
  - SPI FLASH

- **Data Security**
  - Supports AES 128/192/256 ECB/CBC/CTR encryption and decryption.
  - Supports SHA256.
  - Supports 5/7/8/16/32-bit CRC check.
  - Supports SPI Flash firmware encryption protection.
  - TRNG (True Random Number Generator).

- **Package**
  - QFN48 5×5 package.

- **Temperature Range**
  - -40° C to 85° C

1.3. Function Block Diagram



Note: Nor Flash and PSRAM are built-in in part of the chip package.

1.4. Pin Assignment

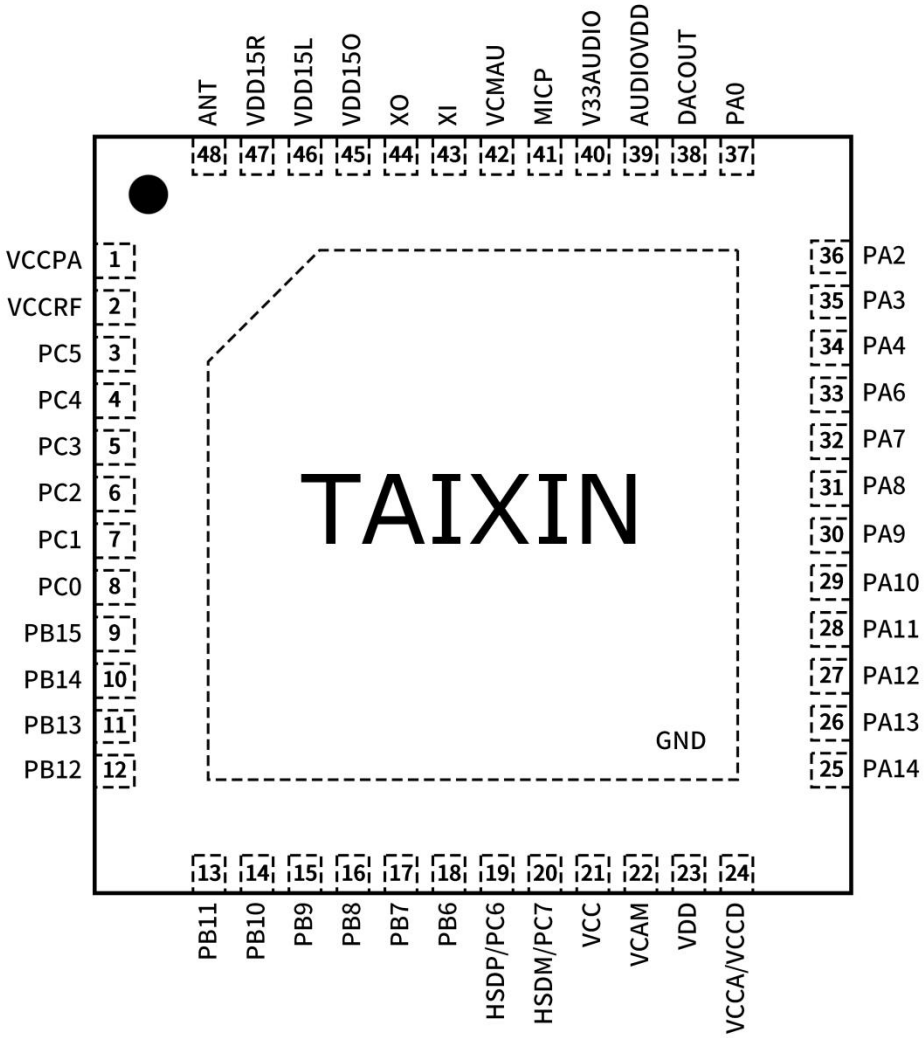


Figure 1-4-1 TXW817-8x0 QFN48 Package Pinout

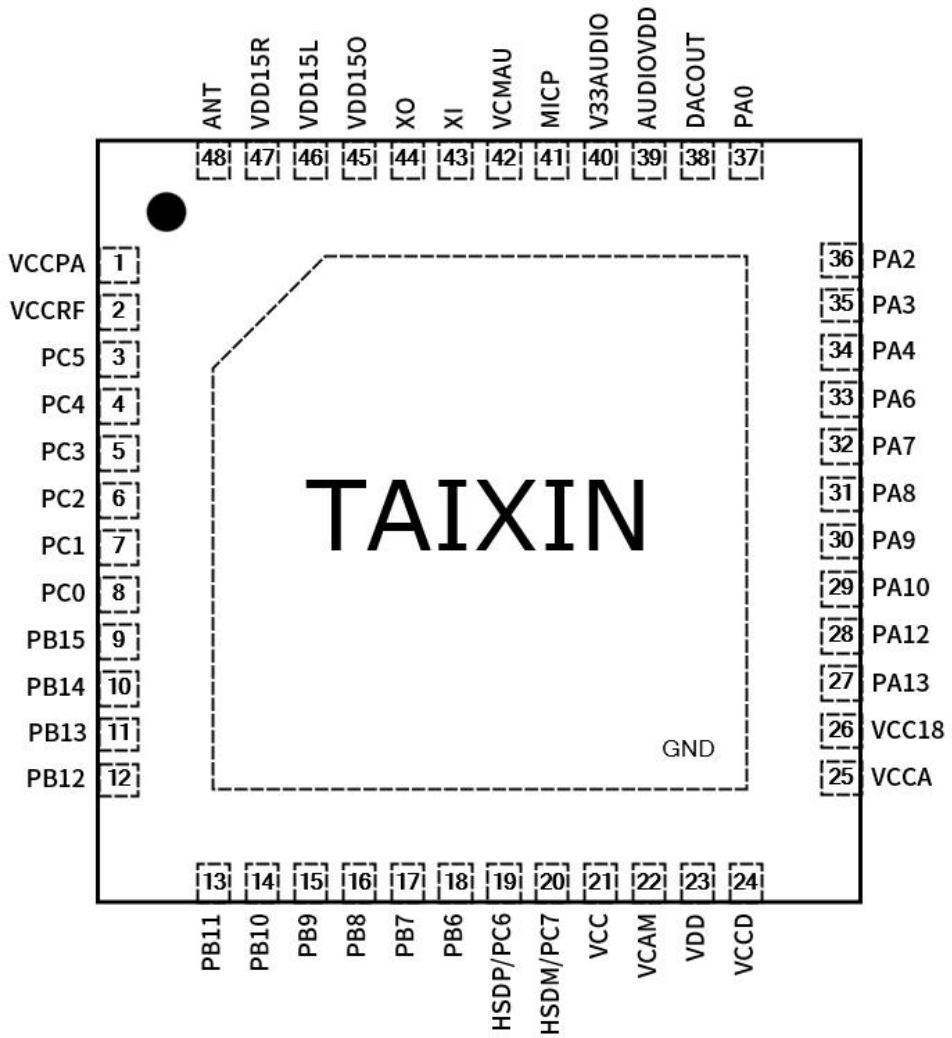


Figure 1-4-2 TXW817-824 QFN48 Package Pinout

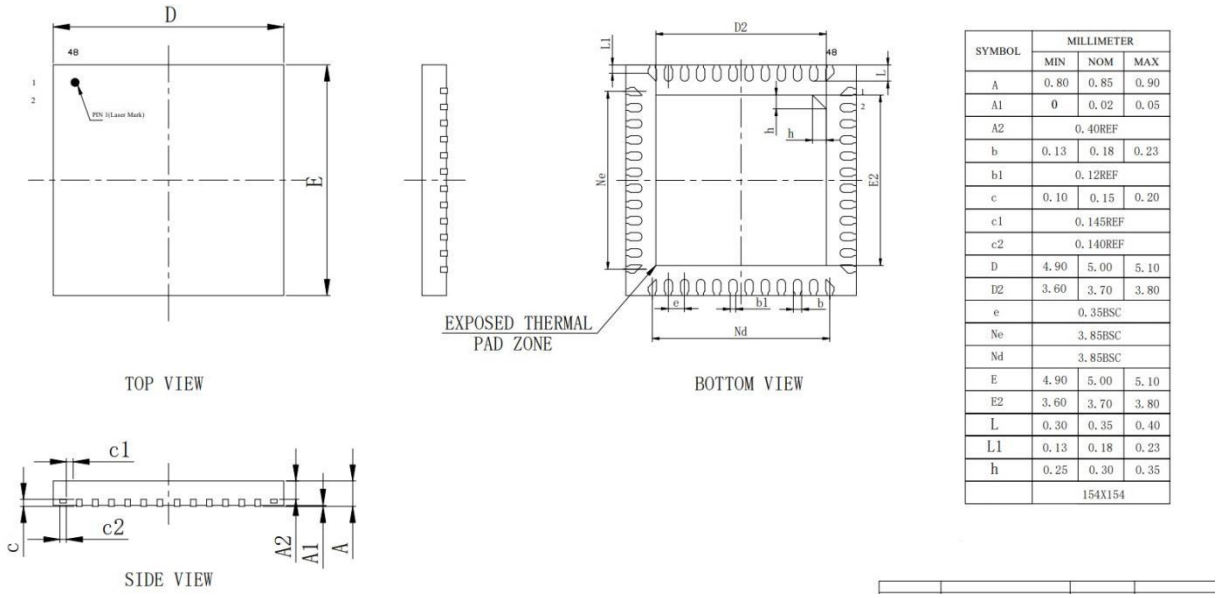
1.5. Package Information

The TXW817 series models are listed in the table below:

Table 1-5-1 Package Information

Model Number	Package	Size	Packaging
TXW817-8x0 TXW817-824	QFN48	5x5	

1.6. Package Dimension Diagram



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
A2		0.40REF	
b	0.13	0.18	0.23
b1		0.12REF	
c	0.10	0.15	0.20
c1		0.145REF	
c2		0.140REF	
D	4.90	5.00	5.10
D2	3.60	3.70	3.80
e		0.35BSC	
Ne		3.85BSC	
Nd		3.85BSC	
E	4.90	5.00	5.10
E2	3.60	3.70	3.80
L	0.30	0.35	0.40
L1	0.13	0.18	0.23
h	0.25	0.30	0.35
	154X154		

Figure 1-6-1 QFN48 POD (Package Outline Diagram)

1.7. Pin Description

1.7.1. Analog Pin Specific Functions

Table 1-7-1-1 Pin Specific Analog Function Table

Pin Number		Pin Name	Pin Type	Pin Description
TXW817-8x0	TXW817-824			
21	21	VCC	AI	Power supply for digital IO, 3.3V; supplies power to PC6 (USBDP), PC7 (USBDM), PA0, PA[2:4], PA[6:14]
23	23	VDD	AI/O	Digital system power supply, default internal LDO output 1.1V. For low-power applications, an external DCDC can be used.
-	26	VCC18	AO	Internal LDO 1.8V output, power supply for internal PSRAM.
24	25	VCCA	AI	Power supply for analog modules, 3.3V.
2	2	VCCRF	AI	Power supply for RF module, 3.3V.
1	1	VCCPA	AI	Power supply for RF PA, 3.3V.
24	24	VCCD	AI	Input power supply for internal VDD LDO. Accepts external power supply of 1.8V - 3.3V. When using internal BUCK, VCCD serves as the feedback pin for the BUCK. If the package does not have a separate VCCD pin, it is internally connected to VCCA. Detailed description is in the hardware design guide.
47	47	VDD15R	AI	RF power supply, 1.8V.
46	46	VDD15L	AI	RF LO power supply, 1.8V.
45	45	VDD15O	AO	Internal LDO output power supply, sourced from VCCA, used to supply power to VDD15L and VDD15R, 1.8V.
22	22	VCAM	AI/O	Internal LDO output or external power supply input; also supplies power to digital IOs PB[6:15] and PC[0:5]. When powered internally, supports 2.5V - 2.8V or 3.3V. When powered externally, supports 1.8V - 3.3V.
42	42	VCMAU	AO	Internal reference output, no load capability.
40	40	V33AUDIO	AI	Power supply for audio module, recommended independent power supply of 3.3V (must be turned off when the device is in sleep mode), or connected to VCAM (2.8 - 3.3V).
39	39	AUDIOVDD	AO	Power supply for audio module, supports internal 2.7V output, used as bias power supply for external analog MIC.
38	38	DACOUT	AO	Audio DAC output.
41	41	MICP	AI	Microphone input P terminal.
43	43	XI	AI	High-speed crystal oscillator input.
44	44	XO	AO	High-speed crystal oscillator output.
48	48	ANT	AI/O	RF antenna port.
GND	GND	EPAD	AI	Ground.

Notes:

1) IOs in the VCAM power domain are only high impedance when VCAM is powered (VCAM is off by default when the chip is powered).
2) Do not use two GPIOs in the same path simultaneously as analog ADCs.
3) Comparator P/N terminals must be used in pairs.

Table 1-7-1-2 Pin Specific Analog Function Table

Pin Name	IO Type	Function Description Default State	Power Domain	ADC Path (Any-end Sampling)	Comparatoe Path （P/N Comparison）	Special Function
HSDP	A	USB	VCC			Digital IO: PC6
HSDM	A	USB	VCC			Digital IO: PC7
PA0	I/O	Input high impedance	VCC	ADKEY_N0	CMP_P0	
PA2	I/O	Input high impedance	VCC			Low-power PWM0
PA3	I/O	Input high impedance	VCC			Low-power PWM1
PA4	I/O	Input high impedance	VCC			
PA6	I/O	Input high impedance	VCC			
PA7	I/O	Input high impedance	VCC			
PA8	I/O	Input high impedance	VCC	ADKEY_N1	CMP_N1	Low-power PWM2
PA9	I/O	Input pull-up 100KΩ	VCC			
PA10	I/O	Input pull-up 100KΩ	VCC			
PA11	I/O	Input high impedance	VCC			Low-power PWM3
PA12	I/O	Input high impedance	VCC			Low-speed oscillator output
PA13	I/O	Input high impedance	VCC			Low-speed oscillator input
PA14	I/O	Input high impedance	VCC			
PB6	I/O	Input high impedance	VCAM	ADKEY_N2	CMP_N2	
PB7	I/O	Input high impedance	VCAM			
PB8	I/O	Input high impedance	VCAM			
PB9	I/O	Input high impedance	VCAM			
PB10	I/O	Input high impedance	VCAM			
PB11	I/O	Input high impedance	VCAM			
PB12	I/O	Input high impedance	VCAM			
PB13	I/O	Input high impedance	VCAM			
PB14	I/O	Input high impedance	VCAM			
PB15	I/O	Input high impedance	VCAM			
PC0	I/O	Input high impedance	VCAM	ADKEY_P0	CMP_P2	
PC1	I/O	Input high impedance	VCAM			
PC2	I/O	Input high impedance	VCAM			

PC3	I/O	Input high impedance	VCAM			
PC4	I/O	Input high impedance	VCAM			
PC5	I/O	Input high impedance	VCAM			

1.7.2. Digital Pin Specific Functions

Table 1-7-2-1 GPIO Pin Specific Digital Function

Pin Name	IO Type	Function Description Default State	Power Domain	Multiplex Function 0	Multiplex Function 1	Multiplex Function 2	Multiplex Function 3
PA0	I/O	Input high impedance	VCC	lcd_data5	lcd_te	rmii_rxd1	lcd_data15
PA2	I/O	Input high impedance	VCC	lcd_data7	qspi_io0	ospi_io0	
PA3	I/O	Input high impedance	VCC	qspi_io1	qspi_io3	ospi_io3	ospi_io1
PA4	I/O	Input high impedance	VCC	lcd_data8	rmii_rxd2	rmii_txd0	lcd_data17
PA6	I/O	Input high impedance	VCC	lcd_data10		rmii_tx_en	lcd_data19
PA7	I/O	Input high impedance	VCC	lcd_data11		ospi_nss0	rmii_crs_dv
PA8	I/O	Input high impedance	VCC	sd_dat0	qspi_clk	ospi_clk	rmii_rx_er
PA9	I/O	Input pull-up 100KΩ	VCC	sd_clk	qspi_io2	ospi_io2	
PA10	I/O	Input pull-up 100KΩ	VCC	sd_cmd	qspi_io1	ospi_io1	
PA11	I/O	Input high impedance	VCC	lcd_data12	qspi_io2	ospi_io2	
PA12	I/O	Input high impedance	VCC	lcd_data13	qspi_io1	ospi_io1	lcd_data20
PA13	I/O	Input high impedance	VCC	lcd_data14	qspi_io0	ospi_io0	lcd_data21
PA14	I/O	Input high impedance	VCC	lcd_data15	qspi_io3	ospi_io3	lcd_data23
PB6	I/O	Input high impedance	VCAM	sd_dat1	dvp_vsync	lcd_data0	lcd_data8
PB7	I/O	Input high impedance	VCAM	sd_dat0	dvp_hsync	lcd_data1	lcd_data9
PB8	I/O	Input high impedance	VCAM	sd_clk	dvp_data_in7	lcd_data2	lcd_data10
PB9	I/O	Input high impedance	VCAM	sd_cmd	dvp_mclk	lcd_data3	lcd_data11
PB10	I/O	Input high impedance	VCAM	sd_dat3	dvp_data_in6	lcd_data4	lcd_data12
PB11	I/O	Input high impedance	VCAM	sd_dat2	dvp_data_in5	lcd_data5	lcd_data13
PB12	I/O	Input high impedance	VCAM	rmii_rxd0	dvp_pixel_clk_in	lcd_data6	lcd_data14
PB13	I/O	Input high impedance	VCAM	rmii_rxd1	dvp_data_in4	lcd_data7	lcd_data15
PB14	I/O	Input high impedance	VCAM	rmii_ref_clkin	dvp_data_in0	lcd_dotclk_or_rwr	lcd_data16
PB15	I/O	Input high impedance	VCAM	rmii_txd0	dvp_data_in3	lcd_hsync_or_dc	lcd_data17
PC0	I/O	Input high impedance	VCAM	rmii_txd1	dvp_data_in1	lcd_vsync_or_cs	lcd_data18
PC1	I/O	Input high impedance	VCAM	rmii_tx_en	dvp_data_in2	lcd_de_or_erd	lcd_data19
PC2	I/O	Input high impedance	VCAM	rmii_crs_dv		lcd_data8	lcd_data20
PC3	I/O	Input high impedance	VCAM	rmii_rx_er		lcd_data9	lcd_data21
PC4	I/O	Input high impedance	VCAM	rmii_rxd2		lcd_data10	lcd_data22
PC5	I/O	Input high impedance	VCAM	rmii_rxd3		lcd_data11	lcd_data23
PC6	I/O	Input high impedance	VCC				
PC7	I/O	Input high impedance	VCC				

1.7.3. Digital Pin Output Arbitrary Mapping Function

Table 1-7-3-1 GPIO Output Function Arbitrary Mapping Table

Function Number	Function Name	Function Description
1	COMP_DOUT_DIG0	Comparator 0 digital IO output
2	comp_dout_dig1	Comparator 1 digital IO output
3	grant_ble_switch_o	Bluetooth coexistence switch signal
4	grant_ble	Bluetooth coexistence BLE arbitration signal
5	grant_Wi-Fi_switch_o	Bluetooth coexistence Wi-Fi switch signal
6	rf_switch_en1	External RF switch enable 1
7	rf_switch_en0	External RF switch enable 0
8	antenna_sel	Dual-antenna selection signal
9	pa_en	External PA enable signal
10	rf_ext_lna_en	External RF LNA enable signal
11	rf_tx_en_fem	External RF FEM transmit enable
12	rf_rx_en_fem	External RF FEM receive enable
13	UART4_tx	UART4 TX output
14	UART5_tx	UART5 TX output
15	UART0_rts_re_o	UART0 RTS RE output
16	UART0_cts_de_out	UART0 RTS DE output
17	UART0_out	UART0 TX output
18	Stmr5_pwm_out	Simple timer5 PWM output
19	Stmr4_pwm_out	Simple timer4 PWM output
20	stmr3_pwm_out	Simple timer3 PWM output
21	stmr2_pwm_out	Simple timer2 PWM output
22	stmr1_pwm_out	Simple timer1 PWM output
23	stmr0_pwm_out	Simple timer0 PWM output
24	tmr3_pwm_out	Timer3 PWM output
25	tmr2_pwm_out	Timer2 PWM output
26	tmr1_pwm_out	Timer1 PWM output
27	tmr0_pwm_out	Timer0 PWM output
28	led_tmr0_pwm_out	LED Timer0 PWM output
29	led_tmr1_pwm_out	LED Timer1 PWM output
30	led_tmr2_pwm_out	LED Timer2 PWM output
31	led_tmr3_pwm_out	LED Timer3 PWM output
32	sdhost_sclk_o	SDC HOST SDCLK output
33	sdhost_cmd_out	SDHOST CMD output
34	sdhost_dat0_out	SDHOST DAT0 output
35	sdhost_dat1_out	SDHOST DAT output
36	sdhost_dat2_out	SDHOST DAT2 output
37	sdhost_dat3_out	SDHOST DAT3 output

38	pdm_mclk	PDM MCLK output
39	qspi_nss1_out	QSPI chip select 1 output
40	spi0_nss_out	spi0 chip select output
41	spi0_sck_out	spi0 CLK output
42	spi0_io0_out	spi0 IO0 output
43	spi0_io1_out	spi0 IO1 output
44	spi0_io2_out	spi0 IO2 output
45	spi0_io3_out	spi0 IO3 output
46	spi1_nss_out	spi1 chip select output
47	spi1_sck_out	spi1 CLK output
48	spi1_io0_out	spi1 IO0 output
49	spi1_io1_out	spi1 IO1 output
50	spi1_io2_out	spi1 IO2 output
51	spi1_io3_out	spi1 IO3 output
52	spi2_nss_out	spi2 chip select output
53	spi2_sck_out	spi2 CLK output
54	spi2_io0_out	spi2 IO0 output
55	spi2_io1_out	spi2 IO1 output
56	spi2_io2_out	spi2 IO2 output
57	spi2_io3_out	spi2 IO3 output
58	iis0_mclk_out	IIS0 MCLK output
59	iis0_wsclk_out	IIS0 WS output
60	iis0_bclk_out	IIS0 BCLK output
61	iis0_do	IIS0 DAT output
62	iis1_mclk_out	IIS1 MCLK output
63	iis1_wsclk_out	IIS1 WS output
64	iis1_bclk_out	IIS1 BCLK output
65	iis1_do	IIS1 DAT output
66	clk_to_io	Clock source IO output
67	LCD_DOTCLK_OR_RWR	LCD display interface DOTCLK/RWR output
68	Lcd_vsync_or_cs	LCD display interface VSYNC/CS output
69	Lcd_hsync_or_dc	LCD display interface HSYNC/DC output
70	Lcd_de_or_erd	LCD display interface DE/ERD output
71	LCD_DAT0	LCD display interface data bit 0 output
72	LCD_DAT1	LCD display interface data bit 1 output
73	LCD_DAT2	LCD display interface data bit 2 output
74	LCD_DAT3	LCD display interface data bit 3 output
75	LCD_DAT4	LCD display interface data bit 4 output
76	LCD_DAT5	LCD display interface data bit 5 output
77	LCD_DAT6	LCD display interface data bit 6 output
78	LCD_DAT7	LCD display interface data bit 7 output
79	LCD_DAT8	LCD display interface data bit 8 output
80	LCD_DAT9	LCD display interface data bit 9 output

81	LCD_DAT10	LCD display interface data bit 10 output
82	LCD_DAT11	LCD display interface data bit 11 output
83	LCD_DAT12	LCD display interface data bit 12 output
84	LCD_DAT13	LCD display interface data bit 13 output
85	LCD_DAT14	LCD display interface data bit 14 output
86	LCD_DAT15	LCD display interface data bit 15 output
87	LCD_DAT16	LCD display interface data bit 16 output
88	LCD_DAT17	LCD display interface data bit 17 output
89	LCD_DAT18	LCD display interface data bit 18 output
90	LCD_DAT19	LCD display interface data bit 19 output
91	LCD_DAT20	LCD display interface data bit 20 output
92	LCD_DAT21	LCD display interface data bit 21 output
93	LCD_DAT22	LCD display interface data bit 22 output
94	LCD_DAT23	LCD display interface data bit 23 output

1.7.4. Digital Pin Intput Arbitrary Mapping Function

Table 1-7-4-1 GPIO Input Function Arbitrary Mapping Table

Function Number	Function Name	Function Description
1	TMR0_CAP_IN	Timer0 capture input
2	TMR0_SYNC_IN/ext_rfswitch_en0_in	Timer0 sync input / External RF switch enable 0 input
3	TMR1_CAP_IN	Timer1 capture input
4	TMR2_CAP_IN	Timer2 capture input
5	TMR3_CAP_IN	Timer3 capture input
6	PDM_DATA_IN	PDM DATA input
7	PTA_REQ_in	PTA REQ input
8	PTA_PRI_in	PTA PRI input
9	FREQ_IND_IN	FREQ IND input
10	STMR0_CAP_IN/LCD_D3_IN	Simple Timer0 capture input / LCD_D3_IN input
11	STMR1_CAP_IN/LCD_D4_IN	Simple Timer1 capture input / LCD_D4_IN input
12	STMR2_CAP_IN/LCD_D5_IN	Simple Timer2 capture input / LCD_D5_IN input
13	STMR3_CAP_IN/LCD_D6_IN	Simple Timer3 capture input / LCD_D6_IN input
14	PORT_WKUP_IN0	IO wake-up channel 0 input
15	PORT_WKUP_IN1/LCD_D7_IN	IO wake-up channel 1 input / LCD_D7_IN input
16	PORT_WKUP_IN2/LCD_D8_IN	IO wake-up channel 2 input / LCD_D8_IN input
17	PORT_WKUP_IN3/LCD_TE	IO wake-up channel 3 input / LCD_TE input
18	UART0_IN	UART0 RX input
19	UART0_CTS_DE_IN	UART0 CTS/DE input
20	UART1_IN/LCD_D9_IN	UART1 RX input / LCD_D9_IN input
21	UART1_CTS_DE_IN/LCD_D10_IN	UART1 CTS/DE input / LCD_D10_IN input

22	FB_IN/EXT_PA_EN/SYS_NMI	FB_IN / EXT_PA enable input / SYS_NMI input
23	UART4_IN	UART4 RX input
24	LCD_D0_IN	LCD_D0_IN input
25	SPI0_NSS_IN	SPI0 NSS input
26	SPI0_SCK_IN	SPI0 SCK input
27	SPI0_IO0_IN	SPI0 IO0 input
28	SPI0_IO1_IN	SPI0 IO1 input
29	SPI0_IO2_IN	SPI0 IO2 input
30	SPI0_IO3_IN	SPI0 IO3 input
31	SPI1_NSS_IN/LCD_D11_IN	SPI1 NSS input / LCD_D11_IN input
32	SPI1_SCK_IN	SPI1 SCK input
33	SPI1_IO0_IN	SPI1 IO0 input
34	SPI1_IO1_IN/LCD_D12_IN	SPI1 IO1 input / LCD_D12_IN input
35	LCD_D1_IN	LCD_D1_IN input
36	LCD_D2_IN	LCD_D2_IN input
37	SPI2_NSS_IN/LCD_D13_IN	SPI2 NSS input / LCD_D13_IN input
38	SPI2_SCK_IN	SPI2 SCK input
39	SPI2_IO0_IN	SPI2 IO0 input
40	SPI2_IO1_IN/LCD_D14_IN	SPI2 IO1 input / LCD_D14_IN input
41	SPI2_IO2_IN/LCD_D15_IN	SPI2 IO2 input / LCD_D15_IN input
42	SPI2_IO3_IN/LCD_D16_IN	SPI2 IO3 input / LCD_D16_IN input
43	STMR4_CAP_IN/LCD_D17_IN	Simple Timer4 capture input / LCD_D17_IN input
44	STMR5_CAP_IN/LCD_D18_IN	Simple Timer5 capture input / LCD_D18_IN input
45	SDHOST_CMD_IN	SDHOST CMD input
46	SDHOST_DAT0_IN	SDHOST DAT0 input
47	SDHOST_DAT1_IN	SDHOST DAT1 input
48	SDHOST_DAT2_IN	SDHOST DAT2 input
49	SDHOST_DAT3_IN	SDHOST DAT3 input
50	IIS0_MCLK_IN/LCD_D19_IN	IIS0 MCLK input / LCD_D19_IN input
51	IIS0_WSCLK_IN/LCD_D20_IN	IIS0 WS input / LCD_D20_IN input
52	IIS0_BCLK_IN/LCD_D21_IN	IIS0 BCLK input / LCD_D21_IN input
53	IIS0_DAT_IN	IIS0 DAT input
54	IIS1_MCLK_IN/UART5_IN/LCD_D22_IN	IIS1 MCLK input / UART5 RX input / LCD_D22_IN input
55	IIS1_WSCLK_IN/LCD_D23_IN	IIS1 WS input / LCD_D23_IN input
56	SPI1_IO2_IN/IIS1_BCLK_IN	SPI1 IO2 input / IIS1 BCLK input
57	SPI1_IO3_IN/IIS1_DAT_IN	SPI1 IO3 input / IIS1 DAT input

2. Function Description

2.1. Processor and Memory

2.1.1. CPU

The TXW817 series chips are equipped with the CK803 processor, with a maximum clock frequency of 240 MHz, featuring the following characteristics:

- Reduced Instruction Set Computer (RISC) architecture
- 32-bit data, with 16-bit/32-bit mixed encoding instructions
- 3-stage pipeline
- 32 KB high-speed cache
- Single-cycle fast hardware multiplier
- Vector interrupt controller and tick timer
- Interrupt response delay of only 13 processor cycles

2.1.2. Memory

The on-chip memory of the TXW817 series chips includes:

- ROM: Contains BOOTLOADER and some kernel functions
- 272 KB SRAM: For data and instruction space
- 54-bit EFUSE: For key storage and customer-defined use

2.1.3. Memory Expansion

The TXW817 series chips support memory expansion, including SPI Flash and PSRAM via the SPI interface (some chips have these integrated). The on-chip QSPI controller supports external QSPI Flash and PSRAM (up to two memory devices can be expanded), with support for XIP (eXecute In Place) functionality. The QSPI supports memory-mapped access to up to 32 MByte of Flash and PSRAM.

2.2. System Clock

The clock sources of the TXW817 series chips include:

- 128 kHz Low-Speed Internal Ring Oscillator (LIRC)
- 10 MHz High-Speed Internal Ring Oscillator (HIRC)
- 32.768KHz low-speed crystal oscillator
- 24~50MHz high-speed crystal oscillator
- 480 MHz fractional PLL for USB2.0
- External IO input clock source

2.3. Analog Peripherals

2.3.1. Analog-to-Digital Converter (SARADC)

The TXW817 series chips integrate one 12-bit comparator and one 12-bit SARADC, which can operate in ADC/DAC mode. The specific characteristics are as follows:

- Supports clock input up to 1 MHz
- Sampling rate up to 62.5 Ksps
- Supports 12-bit ADC/DAC conversion precision
- Supports conversion triggered by Basic Timer 0/1/2/3, Simple Timer 0/1/2/3/4/5, and software-triggered ADC

2.3.2. Temperature Sensor

The TXW817 series chips integrate a temperature sensor. The sensor's voltage is sampled through an internal ADC channel, and the internal temperature of the chip is calculated from the sampled data.

2.3.3. USB2.0

The TXW817 series chips feature an integrated USB2.0 Controller and USB2.0 PHY, compatible with standard USB2.0 High/Full Speed Host & Device protocols (Host supported in some packages). The high-performance USB2.0 PHY includes an innovative CDR (Clock and Data Recovery) patent technology, ensuring reliable operation even in harsh environments. It supports high-speed mode without an external USB2.0 PHY, with a theoretical rate of up to 480 Mbps. It also supports crystal-less USB. When USB2.0 functionality is not required, the pins can be used as two GPIOs.

2.3.4. XOSC

The TXW817 series chips integrate a high-speed crystal oscillator circuit module, requiring an external passive crystal oscillator in the range of 24 - 50 MHz.

2.3.5. PLL

The TXW817 series chips integrate a high-performance 480 MHz fractional PLL for USB2.0.

2.3.6. Audio ADC

The TXW817 series chips feature one delta-sigma audio ADC with the following characteristics:

- Supports sampling rates of 8/11.025/12/16/22.05/24/32/44.1/48 kHz
- Supports single-ended and differential input high-performance analog microphones with built-in PGA
- Supports acoustic echo cancellation
- Supports G.711 A-law encoding and decoding
- Supports Voice Activity Detection (VAD) event generation

2.3.7. Audio DAC

The TXW817 series chips feature one integrated delta-sigma audio DAC.

2.4. Digital Peripherals

2.4.1. GPIO

The TXW817 series chips integrate up to 31 general-purpose GPIOs with the following characteristics:

- Configurable pull-up resistors with values of 4.7KΩ and 100KΩ.
- Pull-down resistor value of 100KΩ.
- Four levels of IO output drive strength are configurable, with ranges of 4/12/20/28mA (each level is 8mA).
- Supports high-level output in open-drain mode.
- Support for latching IO states after power-off in low-power mode.
- Support for ADC analog input function.
- Support for independent digital IO input and output direction enable, and disabling digital IO input/output functions.

2.4.2. SPI/IIC

The TXW817 series chips integrate three SPI interfaces. SPI0/1 support both SPI master and slave modes, while SPI0 supports only SPI functionality and SPI1/2 support both SPI and IIC functions. Their characteristics are as follows:

SPI Features:

- Support for master and slave modes
- Support for Motorola SPI
- Support for master/slave half-duplex transmission

- Programmable serial clock polarity and phase
- Support for four modes:
  - Standard mode: SCLK, CS, IO0 (MOSI), IO1 (MISO), with 1 bit transmitted per SCLK.
  - 3-wire mode: SCLK, CS, IO0, with 1 bit transmitted per SCLK.
  - DUAL mode: SCLK, CS, IO0, IO1, with 2 bits transmitted per SCLK.
  - QUAL mode: SCLK, CS, IO0, IO1, IO2, IO3, with 4 bits transmitted per SCLK.
- Transmission completion flag with MCU interrupt.
- Support for master mode baud rates up to half the system clock.
- Support for 1–32-bit data width.
- Support for DMA (Direct Memory Access).
- Support for transmitting most significant bit (MSB) first or least significant bit (LSB) first.

IIC Module Features:

- Support for master and slave modes.
- Support for master clock synchronization and arbitration.
- Support for slaves to hold down SCL when data is not ready for transmission or the receive buffer is full.
- Support for 7-bit or 10-bit slave addresses.
- Support for DMA.

2.4.3. UART

The TXW817 series chips integrate three UARTs, including two simple UARTs (UART4/5) and one advanced UART0. The characteristics of UART0 are as follows:

- Support for 8-bit and 9-bit data modes.
- Support for parity checking.
- Four-frame receive buffer and one-frame transmit buffer.
- Support for receive and transmit DMA.
- Support for hardware flow control, with enable signals for RTS_N and CTS_N, configurable to assert RTS_N when there are N (N=0, 1, 2, 3) data frames in the receive buffer.
- Hardware detection of receive timeout, with a timeout range of 1–65536 bit times.
- Support for RS485 mode.

The specific features of UART4/5 are as follows:

- Support for half-duplex communication.
- Support for transmitting 9-bit data.
- Support for software parity checking.

2.4.4. IIS_PCM

The TXW817 series chips integrate two IIS_PCM modules for audio application expansion,

with the following characteristics:

- Support for IIS/left-aligned/right-aligned/PCM format transmission.
- Support for left-channel/right-channel/stereo modes.
- Support for master and slave modes.
- Support for 2–32-bit working data width.
- Support for outputting MCLK mode and using the input MCLK as the clock for master and slave devices.
- Support for swapping left and right channels.
- Support for automatic switching between dual addresses.

2.4.5. PDM

The TXW817 series chips integrate one PDM module for audio application expansion. The PDM module is an audio interface for processing digital MEMS microphones, providing high-precision output clocks and supporting left/right-channel and stereo modes. The specific functions are as follows:

- Support for converting PDM data from digital MEMS microphones to 16-bit PCM data.
- Support for left-channel/right-channel/stereo modes.
- Support for two decimation ratios of 50/100 between PDM and PCM modes.
- Support for swapping left and right channels.
- Support for automatic switching between dual addresses with DMA.

2.4.6. Camera DVP Interface

The TXW817 series chips integrate one CMOS Sensor DVP interface module for external camera connection, with the following characteristics:

- Support for 8-bit parallel interface with sensors.
- Support for selecting the polarity of HSYNC and VSYNC.
- Support for invalidation judgment of HSYNC and VSYNC.
- Support for data formats: YUV422 and RAW DATA.

2.4.7. VPP Image Processing Module

- Support for adjusting the order of YUV data.
- Support for retaining only Y data.
- Support for limiting the range of YUV data.
- Support for downsampling YUV images by 1/2 or 1/3.
- Support for Scatter DMA (only for YUV format).
- Support for timestamp watermarking, color framing, and motion detection.

2.4.8. PRC Data Processing Module

- Support for rearranging YUV422 data.
- Hardware acceleration for optical flow algorithms.
- Support for Scatter DMA.

2.4.9. Motion JPEG Video Encoder/Decoder

The TXW817 series chips integrate one MJPEG video encoder and one MJPEG video encoder/decoder for compressing and decompressing images or videos, with the following characteristics:

- Supported maximum resolutions:
  - 8000×8000 at 2fps (photo mode)
  - 4000×4000 at 5fps (photo mode)
  - 1920×1080 at 30fps
  - 1280×720 at 60fps
  - 640×480 at 120fps
- Support for JPEG0/1 encoding with YUV420 pixel data format.
- Support for JPEG1 decoding with YUV420/422 pixel data format.
- Support for dual-buffering of compressed data.
- Support for dynamic adjustment of DQT (Discrete Cosine Transform Quantization Table).
- Support for encoding/decoding JPEG headers.
- Support for Gather DMA.

2.4.10. LCD

The TXW817 series chip integrates one LCD display interface controller and video post-processing hardware module with the following features:

- Support for RGB and MCU (8080 & 6800) interfaces.
- Support for image scaling, 90/180/270-degree rotation, and horizontal and vertical mirroring.
- Support for image OSD (On-Screen Display) and alpha blending.
- Support for CCM (Color Correction Matrix), gamma correction, saturation, and contrast adjustment.
- Support for 2D-GDMA.

2.4.11. Video Data Path

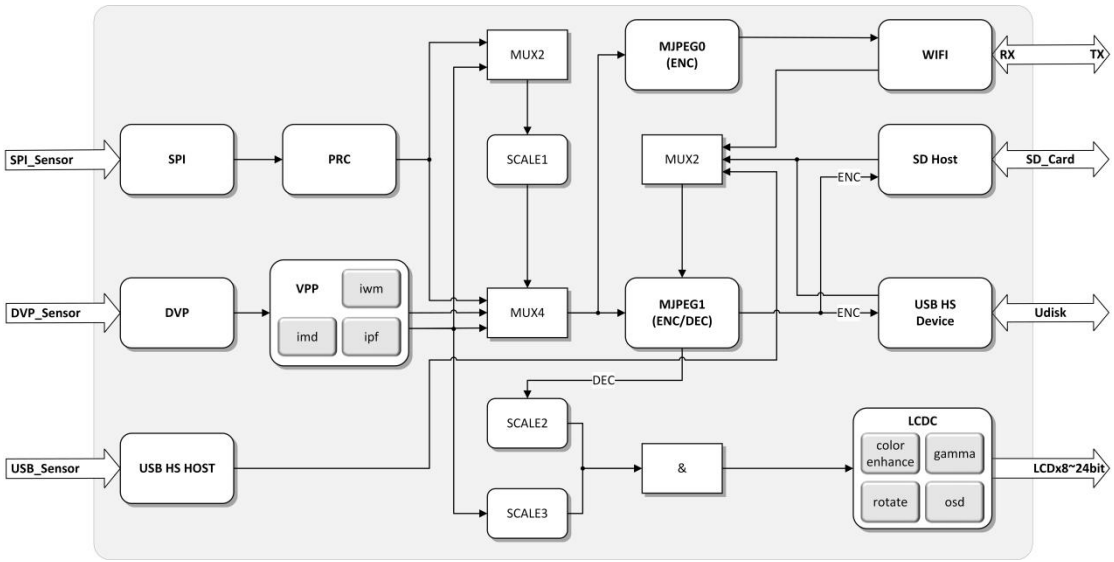


Figure 2-4-9-1 Data Flow Architecture Diagram of Video Codec and Display Subsystem

2.4.12. Ethernet Controller MAC

The TXW817 series chips integrate one MAC function module for expanding Ethernet wired connections. The specific characteristics are as follows:

- Supports 10/100 Mbps.
- Supports RMII interface.
- Supports half-duplex and full-duplex modes.
- Supports up to 16 MAC address filters.
- Supports “ring” descriptor structure.
- Complies with the IEEE 802.3 CSMA/CD standard.

2.4.13. SDIO2.0 Device Controller

The TXW817 series chips integrate one SDIO2.0 Device controller function module, supporting SD 1/4-bit mode and SDIO SPI mode. The clock supports up to 50 MHz. It is used for connecting and expanding Wi-Fi applications through the host SDIO host interface.

2.4.14. SD HOST Controller

The TXW817 series chips integrate one SD host controller function module, supporting SD 1/4-bit mode with a clock up to 50 MHz. It is used for expanding external SD memory cards or SDIO device interface devices.

2.4.15. M2M DMA Module

The TXW817 series chips integrate two memory-to-memory DMA controller function modules for DMA data transfer between internal SRAMs. The specific characteristics are as follows:

- Supports byte alignment.
- Supports up to 64 KB per transfer.
- Supports memcpy and memset modes.
- Supports a 4-word cache buffer.
- Supports transfer completion flags and interrupts.

2.5. Timer Resources

2.5.1. Basic Timers

The TXW817 series chips integrate four normal timers, among which timer0 and timer3 are 32-bit timers, while timer1 and timer2 are 16-bit timers with DMA and infrared functions. Below is an explanation using the 16-bit counter timer1; timer0 and timer3 correspondingly have various bit-width definitions set to 32 bits.

Timer1 consists of a 16-bit auto-reload counter that can measure the pulse width of an input signal (input capture) or generate output waveforms (output compare, PWM, etc.). The main features are:

- 16-bit up-counter.
- Programmable (can be modified in real-time) prescaler, supporting up to 128x division.
- Supports selecting GPIO as the counting clock source.
- Supports different counting clock sources.
- Allows updating the timing period register after each counter cycle.
- Supports input capture function:
  - Supports saving up to one capture event pointer simultaneously.
  - Each capture event polarity can be configured independently.
  - Configurable whether to reset the counter value upon each capture event.
- PWM output
- Supports automatic reload of period and duty cycle.
- Uses external signals to control timer synchronization and inter-timer synchronization circuits.
- Supports infrared functions.

2.5.2. Simple Timers

The TXW817 series chips integrate one simple timer module, composed of stimer0, stimer1, stimer2, stimer3, stimer4, and stimer5, totaling six 32-bit basic function timers. It supports

multiple counting clock source selections and various working modes, including timer mode, counter mode, capture mode, and PWM mode.

2.5.3. Watchdog Timer

The TXW817 series chips integrate an independent watchdog module that operates separately from the system to reset and restart the system in case of abnormal system events. The watchdog module operates on a 32 kHz clock, which is a 2x division of the 64 kHz low-speed RC clock, independent of the system clock. The default configuration is to reset the system every 2 seconds. Therefore, in user programs, the watchdog must be fed (reset) before it triggers a system reset to restart the timer. Users can configure the watchdog reset interval from 8 ms to 256 s. The working mode can be set to generate an interrupt or directly reset the system.

2.6. Security Hardware Accelerators

2.6.1. CRC Module

The TXW817 series chips integrate one CRC function module for data verification. The specific characteristics are as follows:

- Supports various polynomial lengths, including 5/7/8/16/32 bits.
- Supports custom-defined polynomials.
- Supports CRC verification for multiple segmented data.

2.6.2. AES Module

The TXW817 series chips integrate one AES function module for data encryption and decryption. The specific characteristics are as follows:

- Supports AES-128/192/256 in ECB/CBC/CTR modes for encryption and decryption.
- Supports DMA mode with a maximum DMA data length of 1 MByte.

2.6.3. SHA Module

The TXW817 series chips integrate a SHA function module for data verification. Features include:

- Supports SHA2-256.
- Supports DMA mode with a maximum DMA data length of 65,536 bytes.
- Supports SHA computation for multiple segmented data.
- Maximum data rate: 700 Mbps @ 240 MHz (system clock).

2.6.4. TRNG Module

The TXW817 series chips integrate one True Random Number Generator (TRNG) module for generating secure random seeds for data security.

3. Electrical Parameters

3.1. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Max	Unit
V_{VCC}	Operating Voltage	-	-0.3	3.6	V
V_{VCCA}	Analog Operating Voltage	-	-0.3	3.6	V
$VCCPA$ $VCCRF$	RF Operating Voltage	-	-0.3	3.6	V
T_{ST}	Storage Temperature	-	-40	150	°C

Note: Operation outside the absolute maximum ratings may cause permanent damage to the chip. Using the chip outside the recommended operating conditions but within the absolute maximum ratings may affect the reliability, functionality, and performance of the chip and may reduce its lifespan.

3.2. Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{VCC}	Operating Voltage	-	3	3.3	3.6	V
V_{VCCA}	Analog Operating Voltage	-	3	3.3	3.6	V
$VCCPA$ $VCCRF$	RF Operating Voltage	-	3	3.3	3.6	V
$VCAM^{(1)}$	Vcam LDO Load Capacity	VCAM = 2.8V		150		mW
$VCC18$	VCC18 LDO Load Capacity	VCC18 = 1.8V		180		mW
T_A	Operating Temperature	-	-40	-	85	°C

Note:

1) The VCAM/VCC18 LDO load capability is specified at an operating temperature of 85°C. The VCAM LDO load capability increases with decreasing temperature, decreases with decreasing VCC voltage, and increases with decreasing VCAM voltage level.
2) For packages with integrated PSRAM, the PSRAM itself consumes approximately 20 mA of the VCC18 LDO load capability.

3.3. DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
CIN	Pin Capacitance	-	2	-	pF
VIH	High-Level Input Voltage	0.7*VCC	-	VCC+0.3	V
VIL	Low-Level Input Voltage	-0.3	-	0.3*VCC	V
IIH	High-Level Input Current	-	-	50	nA
IIL	Low-Level Input Current	-	-	50	nA
VOH	High-Level Output Voltage	0.9*VCC	-	-	V
VOL2	Low-Level Output Voltage	-	-	0.1*VCC	V
IOH	High-Level Output Current (VCC = 3.3V, VOH >= 2.64V, PAD_DRIVER = 3)	-	28	-	mA
IOL	Low-Level Output Current (VDD1 = 3.3V, VOL = 0.5V, PAD_DRIVER = 3)	-	50	-	mA
RPU	Pull-Up Resistor	4.7	100	100	kΩ
RPD	Pull-Down Resistor		100		kΩ
VIH_nRST	Chip MCLR Reset Release Voltage	0.7*VCC	-	VCC+0.3	V
VIL_nRST	Chip MCLR Reset Voltage	-0.3	-	0.3*VCC	V

Note:

1. VOH and VOL are measured under high-impedance load conditions.

3.4. AC Electrical Characteristics

3.4.1. External Clock Source Characteristics

Symbol	Parameter	Condition	Minimum Value	Typical Value	Maximum Value	Unit
f_{xoscm}	User External Clock Frequency			40		MHz

V_{BIAS}	XOSCI/XOSCO Bias Level	-	-	550	-	mV
V_{xoh}	XOSCI Input Pin High-Level Voltage	-	-	0.77	-	V
V_{xol}	XOSCO Input Pin Low-Level Voltage	-	-	0.33	-	V
$Duty_{(xoscm)}$	Duty Cycle	-	42	-	58	%
ACC_{xoscm}	HSE Accuracy	-	-	-	-	ppm
$t_{SU(xoscm)}$	Start-up Time	-	-	5		ms
$I_{VCCA(XOSCM)}$	XOSCM Oscillator Power Consumption	Average Power	-	0.7	-	mA

3.4.2. Internal Clock Source Characteristics

Table 3-4-2-1 RC10M Oscillator Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{VCCA}	Supply Voltage	-	3	3.3	3.6	V
RC10M	Frequency	Tested after 25°C trim	9	10	11	MHz
ACC_{RC10M}	RC10M Oscillator Accuracy	-40°C ~ 85°C	-6	-	+6	%
$t_{SU(RC10M)}$	RC10M Oscillator Start-Up Time	-	-	60	-	us
$I_{VCCA(RC10M)}$	RC10M Oscillator Power Consumption	Average Power	-	-	1	mA

Table 3-4-2-2 RC128K Oscillator Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
RC128K	Frequency	TA=25°C	-	128	-	kHz
$I_{DD(RC128K)}$	RC128K Oscillator Power Consumption	-	-	-	-	uA

3.5. Power Consumption Characteristics

3.5.1. RF Power Consumption

The following power consumption data is based on tests conducted at a supply voltage of 3.3V, ambient temperature of 25°C, and CPU running at 120MHz. All transmission data are measured at 100% duty cycle.

RF Power Consumption (100% Duty Cycle Measured)			
Operating Mode	**Description**		**Average(mA)**
Active (LDO Mode)	TX	802.11g, 20 MHz, 54 Mbps, 15dBm	240
		802.11n, 20 MHz, MCS7, 15dBm	240
		802.11n, 20 MHz, MCS7, 6dBm	168
	RX	802.11b/g/n, 20 MHz	76

The following power consumption data are estimated:

RF Power Consumption (50% Duty Cycle Estimated)			
Operating Mode	**Description**		**Average(mA)**
Active (LDO Mode)	TX+RX	802.11g, 20 MHz, 54 Mbps, 15dBm	158
		802.11n, 20 MHz, MCS7, 15dBm	158
		802.11n, 20 MHz, MCS7, 6dBm	122

3.5.2. CPU Power Consumption

MCU State	WLAN State	TX/RX	Test Conditions		Power Consumption
$LP^{(1)}$	OFF	-	Always-on power domain logic active, 272KB SRAM not powered off	-	233.5uA
	OFF	-	Always-on power domain logic active, 16KB SRAM not powered off	-	31.3uA
$ULP^{(1)}$	OFF	-	-	-	28.1uA
Chip Off	-	-	CHIP_EN = 0	-	0.7uA

Note: Only IO and internal RC wake-up are supported.

3.6. Reliability

3.6.1. ESD Electrical Characteristics

Symbol	Parameter	Test Conditions	Maximum	Unit	Level
ESD	Electrostatic Discharge (Human Body Model, HBM)	TA = + 25°C, JEDEC EIA/JESD22-A114	2000	V	-
	Electrostatic Discharge (Charged Device Model, CDM)	TA = + 25°C, JEDEC EIA/JESD22-C101-B	1000	V	-

3.6.2. Latch-Up Electrical Characteristics

Symbol	Parameter	Test Conditions	Test Type	Minimum	Unit
LU	Static latch-up class	JEDEC STANDARD NO.78D	Class I (TA = +25 °C)	±200	mA

3.7. Wi-Fi RF Performance and Power Consumption

3.7.1. Wi-Fi Transmitter Performance

Parameter	Condition	Typical Value(dBm)
Output Power	802.11g, 20 MHz, 54 Mbps	16
	802.11n, 20 MHz, MCS7	16

3.7.2. Wi-Fi Receiver Performance

Parameter	Condition	Typical Value(dBm)
Receiver Sensitivity	HT20 MCS7 4k	-72.5
	NONHT 54M	-74.5
	NONHT 6M	-89.5
	CCK11M	-85

	CCK5.5M	-88
	DSSS2M	-91.5
	DSSS1M	-96

3.7.3. BLE Transmitter Performance

Parameter	Conditions	Typical Value (dBm)
Output Power		20

3.7.4. BLE Receiver Performance

Parameter	Conditions	Typical Value (dBm)
Receive Sensitivity	1Mbps	-94.5

3.8. Audio Performance

3.8.1. Audio ADC Performance

Parameter	Conditions	Typical Value (dBm)
SNR	1KHz silent file, sample rate = 44.1KHz, encoding rate = 44.1*16Kbps	81
THD+N	1KHz silent file, sample rate = 44.1KHz, encoding rate = 44.1*16Kbps	-78

3.8.2. Audio DAC Performance

Parameter	Conditions	Typical Value (dBm)
SNR	1KHz silent file, sample rate = 44.1KHz, encoding rate = 44.1*16Kbps	82
THD+N	1KHz silent file, sample rate = 44.1KHz, encoding rate = 44.1*16Kbps	-75

4. Reference Design

5. Ordering Information

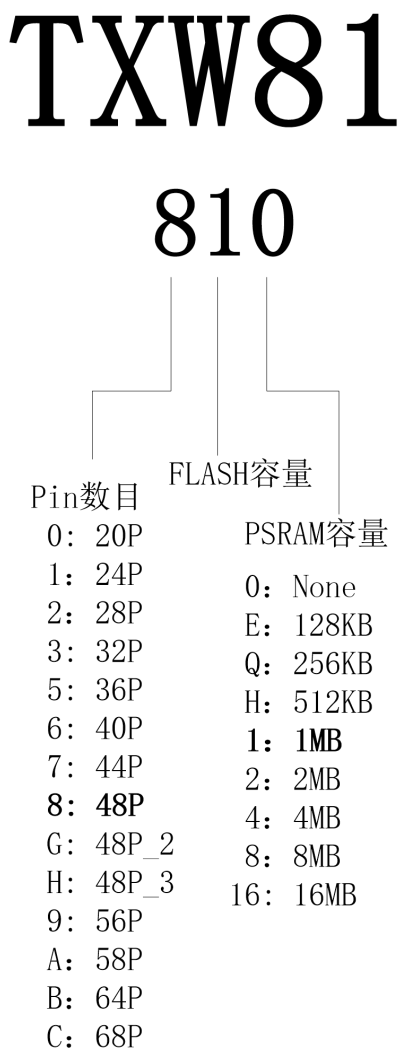


Figure 5-1 Model Naming

Table 5-1 Ordering Information

Product Number	Package	Size	Description
TXW817-810	QFN48	5x5	Built-in 8Mbit FLASH, for video + audio applications, supports USB High-Speed Device.
TXW817-824	QFN48	5x5	Built-in 16Mbit FLASH + 32Mbit PSRAM, for video + audio applications, supports USB High-Speed Device & Host.